AN10951

1805 MHz to 1880 MHz asymmetrical Doherty amplifier with the BLF7G20LS-90P and BLF7G21LS-160P

Rev. 1 — 10 December 2010 Application note

Document information

Info	Content
Keywords	Doherty architecture, Digital PreDistortion (DPD), IS-95, multi-carrier GSM, W-CDMA, pulse, BLF7G20LS-90P, BLF7G21LS-160P
Abstract	This application note describes the design and performance of an asymmetrical Doherty amplifier in the 1805 MHz to 1880 MHz band using the BLF7G20LS-90P and the BLF7G21LS-160P LDMOS transistors.

Revision history

Rev	Date	Description
1	20101210	Initial version

Contact information

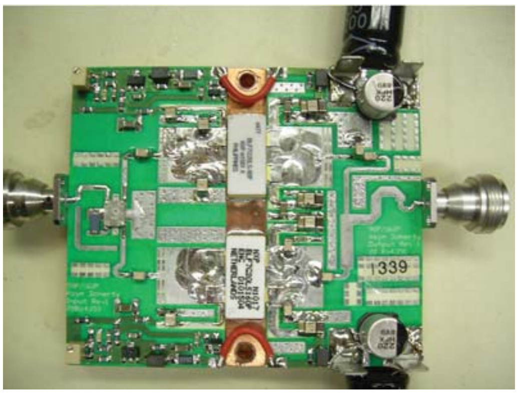
For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

This application note describes the design and performance of an asymmetrical Doherty amplifier in the 1805 MHz to 1880 MHz band using the BLF7G20LS-90P and the BLF7G21LS-160P LDMOS transistors.

The asymmetrical Doherty amplifier design uses NXP Semiconductors' seventh generation push-pull LDMOS transistors BLF7G20LS-90P and BLF7G21LS-160P on a 0.51 mm (0.020") thick Rogers 4350, Printed-Circuit Board (PCB). The BLF7G20LS-90P is rated at 90 W and operates as the main amplifier for the carrier signal. The BLF7G21LS-160P is rated at 160 W and operates as the amplifier for peak signals. Both devices are internally matched at the input and output.



019aaa400

Fig 1. The assembled asymmetrical Doherty amplifier

2. Test summary

Amplifier under test: board number: 1339; date code m1001/D101504; Rogers 4350 PCB, thickness of 0.51 mm (0.020").

The amplifier was characterized under the following conditions:

- Frequency band: 1805 MHz to 1880 MHz
- Network analyzer measurements for gain (G_p), delay (t_d) and Input Return Loss (IRL) at:
  - output power (P_L) = 46 dBm
  - drain-source voltage (V_{DS}) = 28 V
  - quiescent drain current (I_{Dq}) (main amplifier) = 350 mA
  - gate-source voltage (V_{GS}) (peak amplifier) = 0.3 V
- Peak output power measurement:
  - using the standard CDMA IS-95 signal, the peak-to-average ratio (PAR) = 9.7 dB at 0.01 % probability on the CCDF to determine output power (P_L)

    where the PAR reaches a value of 6.7 dB at 0.01 % probability on the CCDF. This is called the 3 dB compression point. V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA and V_{GS} (peak amplifier) = 0.3 V

- using a pulsed signal and measuring the 1 dB and 3 dB compression points with a pulse width of 12 μs at 10 % duty cycle: V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA and V_{GS} (peak amplifier) = 0.3 V

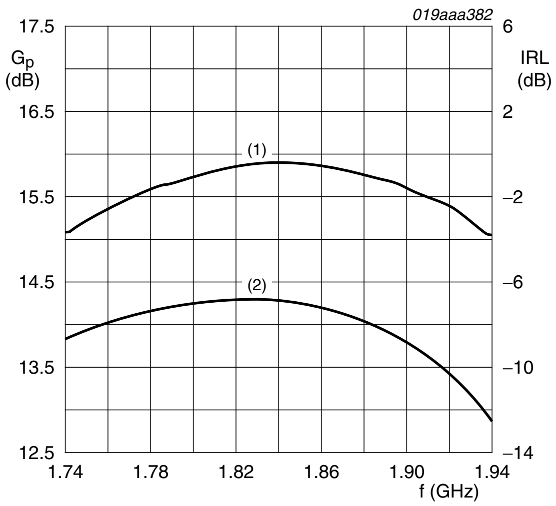
- IS-95 measurement at V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA and V_{GS} = 0.3 V
- 6-carrier GSM measurements using a 6-carrier GSM signal with a 4 MHz spacing, PAR = 7.5 dB at 0.01 % probability: V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA and V_{GS} (peak amplifier) = 0.3 V
- Digital PreDistortion (DPD) measurements using a DPD system:
  - 2-carrier W-CDMA signal, 10 MHz spacing, peak-to-average ratio (PAR) = 7.6 dB at 0.01 % probability (total signal), V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA and V_{GS} (peak amplifier) = 0.3 V
  - 2-carrier LTE signal, 10 MHz spacing, 10 MHz carrier bandwidth, peak-to-average ratio (PAR) = 7.6 dB at 0.01 % probability (total signal), V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA, V_{GS} (peak amplifier) = 0.3 V

3. RF Performance

3.1 Network analyzer measurements

Network analyzer measurements were performed under the following conditions:

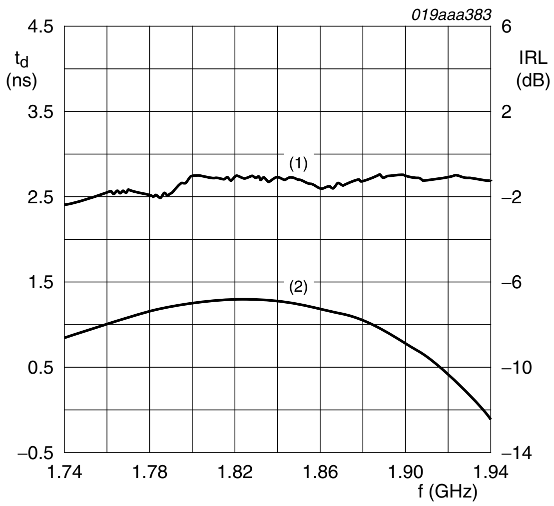
- P_L = 46 dBm
- V_{DS} = 28 V
- I_{Dq} (main amplifier) = 350 mA
- V_{GS} (peak amplifier) = 0.3 V



(1) G_p.

(2) IRL.

Fig 2. Power gain and input return loss as a function of frequency



(1) t_d.

(2) IRL.

Fig 3. Delay time and input return loss as a function of frequency

3.2 Peak output power measurements

Two methods were used to measure peak output power.

- Using a standard IS-95 signal (PAR = 9.7 dB at 0.01 % probability on the CCDF), to determine the output power when PAR reaches 6.7 dB at 0.01 % probability on the CCDF, measured as the 3 dB compression point
- Using the pulsed signal (12 μs width and 10 % duty cycle), measuring the 1 dB and 3 dB compression points

The peak output power measurements were performed under the following conditions:

- Bias: V_{DS} = 28 V
- I_{Dq} (main amplifier) = 350 mA
- V_{GS} (peak amplifier) = 0.3 V

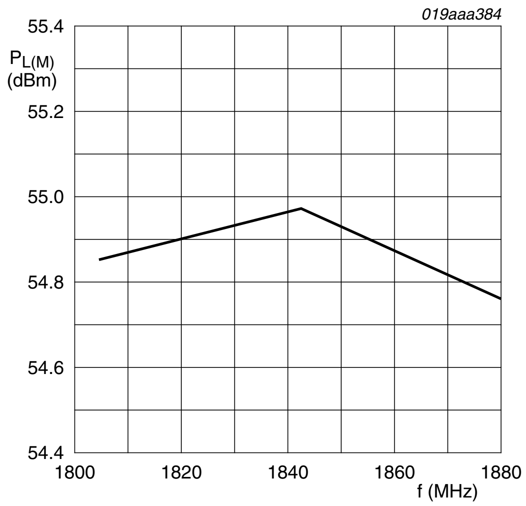
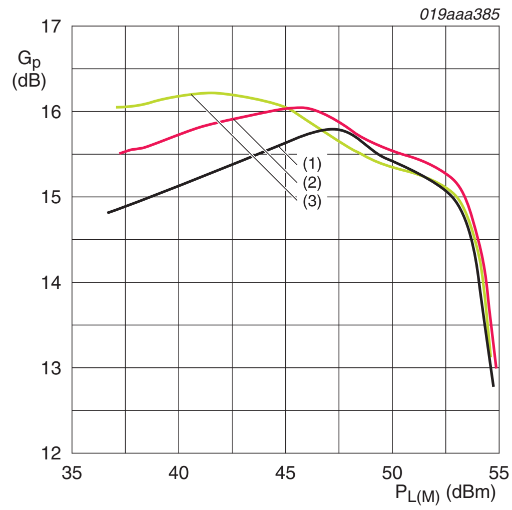


Fig 4. Peak output power as a function of frequency



(1) f = 1805 MHz.

(2) f = 1842.5 MHz.

(3) f = 1880 MHz.

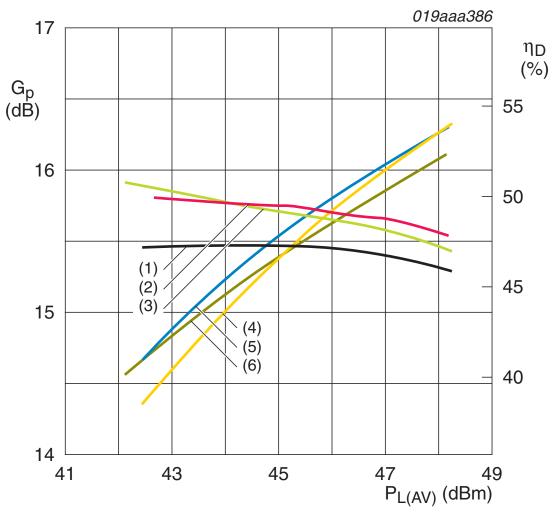
Fig 5. Power gain as a function of peak output power

3.3 IS-95 measurements

The IS-95 measurements were performed under the following conditions:

- Bias: V_{DS} = 28 V
- I_{Dq} (main amplifier) = 350 mA
- V_{GS} (peak amplifier) = 0.3 V

Remark: When calculating the drain efficiency, the increase in current caused by the gate temperature compensation circuit (≅ 50 mA) must be subtracted from the drain current value. This is approximately 50 mA.



(1) G_p at 1805 MHz.

(2) G_p at 1842.5 MHz.

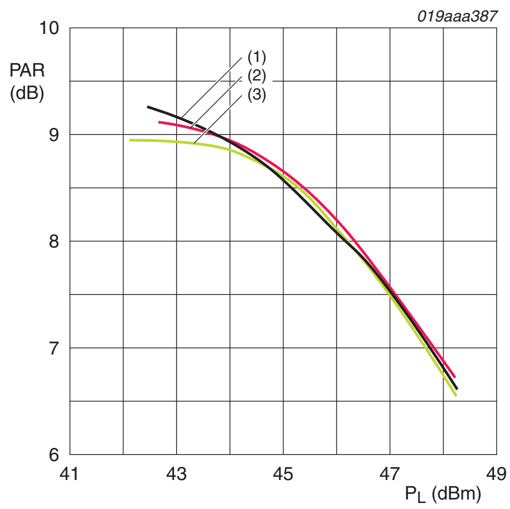
(3) G_p at 1880 MHz.

(4) η_D at 1805 MHz.

(5) η_D at 1842.5 MHz.

(6) η_D at 1880 MHz.

Fig 6. Power gain and drain efficiency as a function of average output power, IS-95



(1) f = 1805 MHz.

(2) f = 1842.5 MHz.

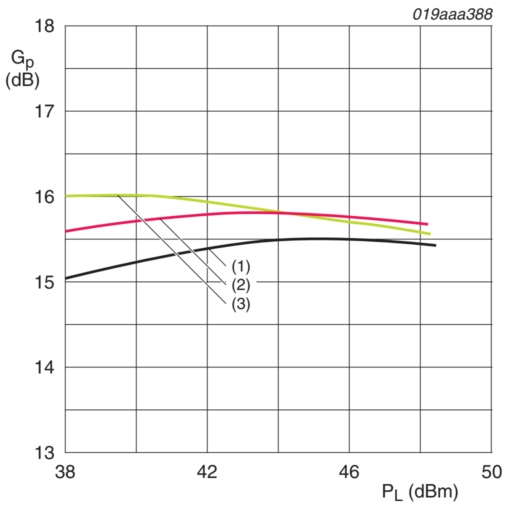
(3) f = 1880 MHz.

Fig 7. PAR as a function of output power

3.4 6-Carrier GSM measurements

The 6-carrier GSM measurements were performed under the following conditions:

- Bias: V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA and V_{GS} (peak amplifier) = 0.3 V
- Test signal: 6 carrier GSM, 4 MHz spacing, PAR = 7.5 dB at 0.01% probability
- IMD3: 4 MHz offset from the closest carrier
- IMD5: 8 MHz offset from the closest carrier

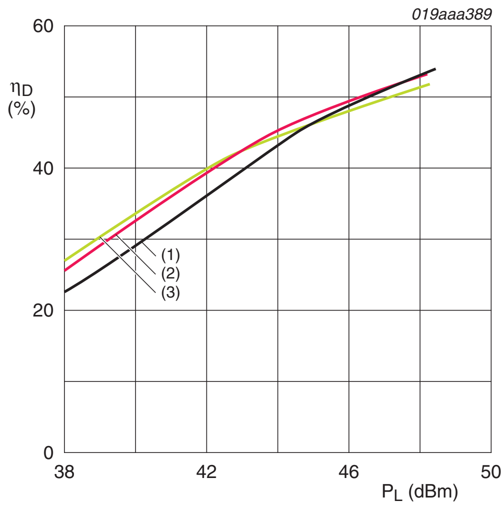


(1) f = 1805 MHz.

(2) f = 1842.5 MHz.

(3) f = 1880 MHz.

Fig 8. Power gain as a function of output power

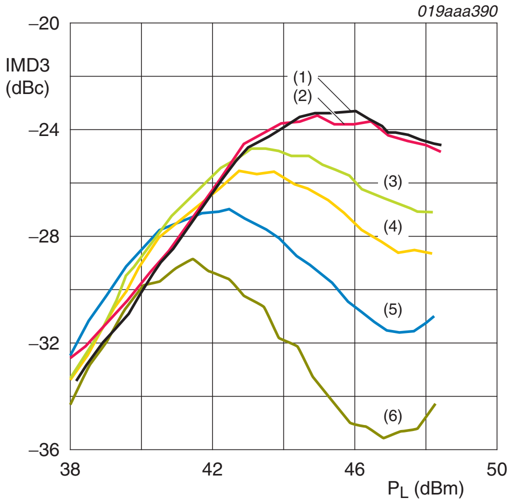


(1) f = 1805 MHz.

(2) f = 1842.5 MHz.

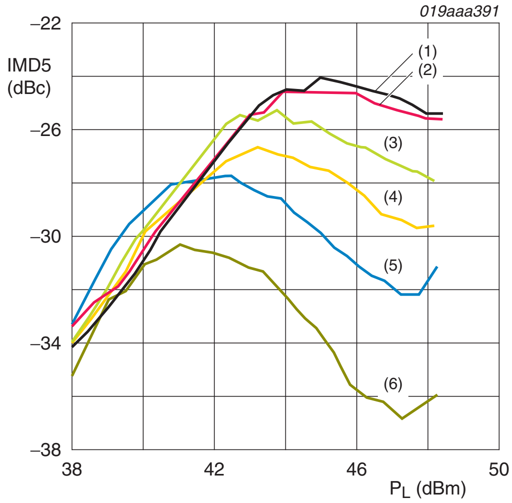
(3) f = 1880 MHz.

Fig 9. Drain efficiency as a function of output power



(1) 1805 MHz IMD3 low.
(2) 1805 MHz IMD3 high.
(3) 1842.5 MHz IMD3 low.
(4) 1842.5 MHz IMD3 high.
(5) 1880 MHz IMD3 low.
(6) 1880 MHz IMD3 high.

Fig 10. IMD3 as a function of output power



(1) 1805 MHz IMD5 low.
(2) 1805 MHz IMD5 high.
(3) 1842.5 MHz IMD5 low.
(4) 1842.5 MHz IMD5 high.
(5) 1880 MHz IMD5 low.
(6) 1880 MHz IMD5 high.

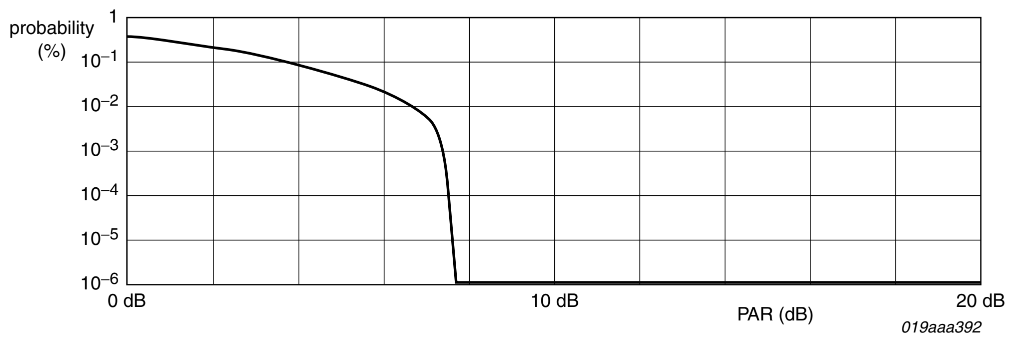
Fig 11. IMD5 as a function of output power

4. DPD Measurements

4.1 DPD measurements with 2-carrier W-CDMA

The DPD measurements were performed using a Texas Instruments DPD system under the following conditions:

- 2-carrier W-CDMA signal, spacing: 10 MHz, peak-to-average ratio (PAR) = 7.6 dB at 0.01 % probability (total signal)
- Channel bandwidth = 3.84 MHz
- IMD: 10 MHz offset from the carrier (IBW = 3.84 MHz)
- V_{DS} = 28 V, I_{Dq} (main amplifier) = 350 mA, V_{GS} (peak amplifier) = 0.3 V
- IBW = 3.84 MHz



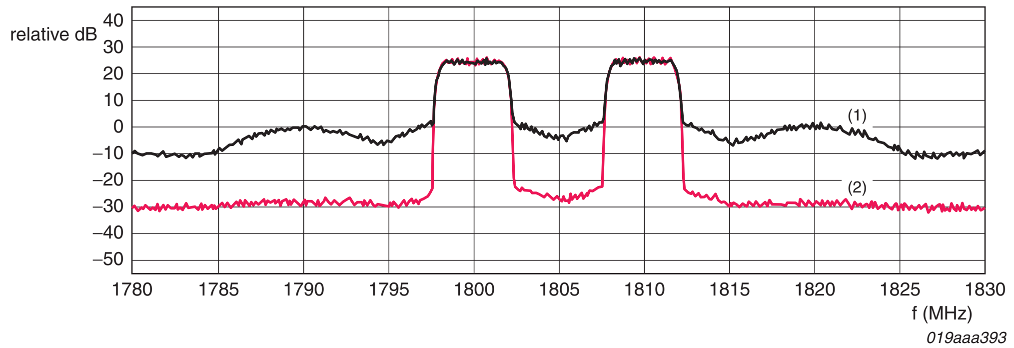
Test signal: 2-carrier W-CDMA, 10 MHz spacing; PAR = 7.6 dB at 0.01% probability.

Fig 12. CCDF test signal

4.1.1 1.805 GHz DPD correction

The following DPD measurements were performed under the following conditions:

- f_c = 1.805 GHz
- P_L = 46.8 dBm
- IMD = 10 MHz offset from the carrier
- Channel bandwidth = 3.84 MHz



(1) IMD uncorrected: −25.4 dBc (lower), −24.9 dBc (upper).

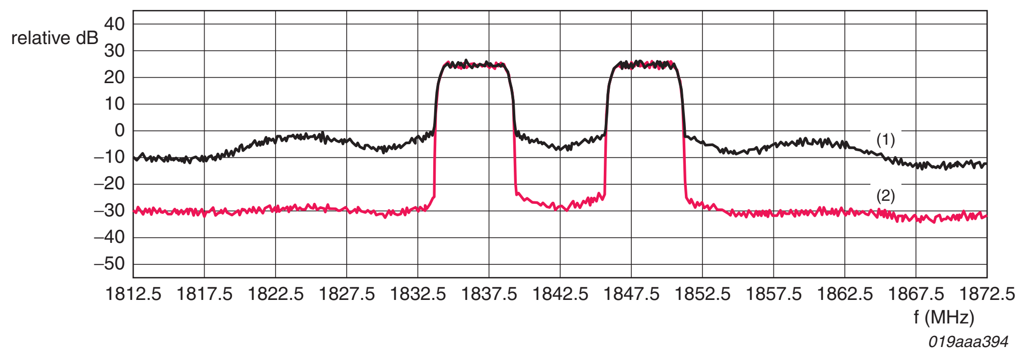
(2) IMD corrected: −53.2 dBc (lower), −53.6 dBc (upper).

Fig 13. DPD measurement, f_c = 1.805 GHz

4.1.2 1.8425 GHz DPD correction

The following DPD measurements were performed under the following conditions:

- f_c = 1.8425 GHz
- P_L = 46.8 dBm
- IMD = 10 MHz offset from the carrier
- IBW = 3.84 MHz



(1) IMD uncorrected: −27.6 dBc (lower), −29.6 dBc (upper).

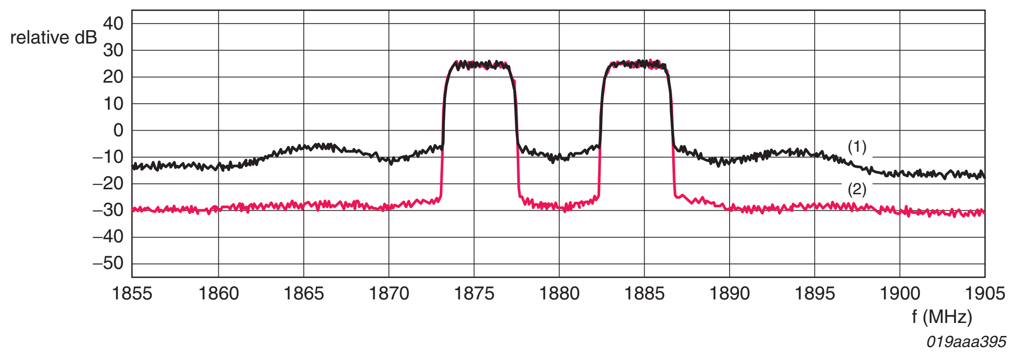
(2) IMD corrected: −54.1 dBc (lower), −55.5 dBc (upper).

Fig 14. DPD measurement, f_c = 1.8425 GHz

4.1.3 1.88 GHz DPD correction

The following DPD measurements were performed under the following conditions:

- f_c = 1.88 GHz
- P_L = 46.8 dBm
- IMD = 10 MHz offset from the carrier
- IBW = 3.84 MHz



(1) IMD uncorrected: −31.3 dBc (lower), −33.3 dBc (upper).

(2) IMD corrected: −52.9 dBc (lower), −53.5 dBc (upper).

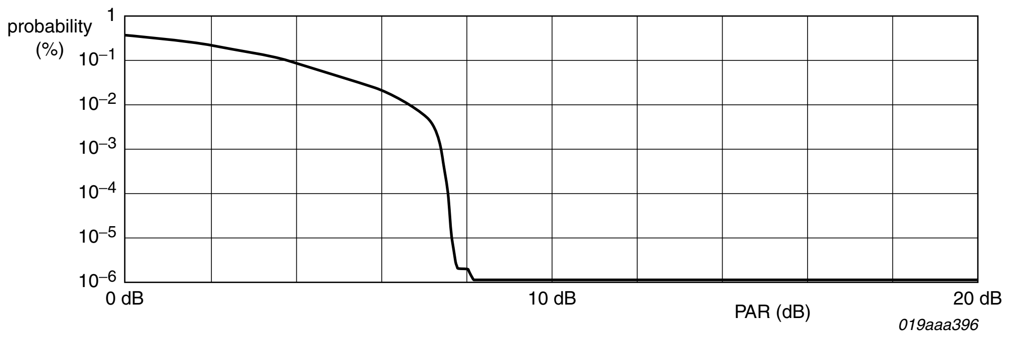
Fig 15. DPD measurement, f_c = 1.88 GHz

4.2 DPD measurements with 2-carrier LTE

The DPD measurements were performed using a Texas Instruments DPD system under the following conditions:

- 2-carrier LTE signal, spacing: 10 MHz, peak-to-average ratio (PAR) = 7.6 dB at 0.01 % probability (total signal)
- Channel bandwidth = 10 MHz
- ACPR: 7.5 MHz offset from the carrier (IBW = 3.84 MHz)

- V_{DS} = 28 V, I_{Dq} (main amplifier) = 500 mA, V_{GS} (peak amplifier) = 0.4 V



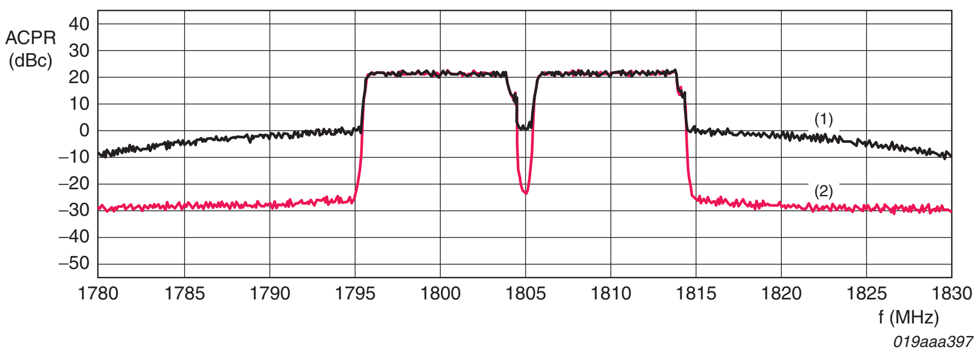
Test signal: 2-carrier W-CDMA, 10 MHz spacing; PAR = 7.6 dB at 0.01% probability.

Fig 16. Test signal CCDF

4.2.1 1.805 GHz DPD correction

The following DPD measurements were performed under the following conditions:

- f_c = 1.805 GHz
- P_L = 46.8 dBm
- Channel bandwidth = 10 MHz
- ACPR: 7.5 MHz offset from the carrier (IBW = 3.84 MHz)



(1) IMD uncorrected: −25.8 dBc (lower), −25.7 dBc (upper).

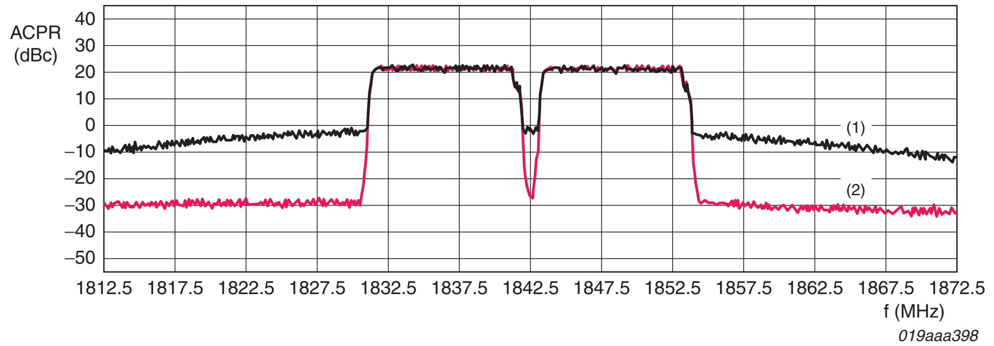
(2) IMD corrected: −51.9 dBc (lower), −52.2 dBc (upper).

Fig 17. DPD measurement, f_c = 1.805 GHz

4.2.2 1.8425 GHz DPD correction

The following DPD measurements were performed under the following conditions:

- f_c = 1.8425 GHz
- P_L = 46.8 dBm
- Channel bandwidth = 10 MHz
- ACPR: 7.5 MHz offset from the carrier (IBW = 3.84 MHz)



(1) IMD uncorrected: −28.1 dBc (lower), −29.7 dBc (upper).

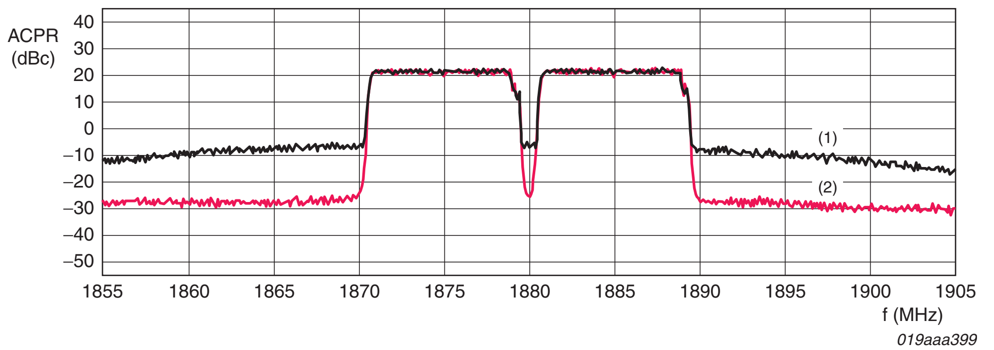
(2) IMD corrected: −54.2 dBc (lower), −55 dBc (upper).

Fig 18. DPD measurement, f_c = 1.8425 GHz

4.2.3 1.88 GHz DPD correction

The following DPD measurements were performed under the following conditions:

- f_c = 1.88 GHz
- P_L = 46.8 dBm
- Channel bandwidth = 10 MHz
- ACPR: 7.5 MHz offset from the carrier (IBW = 3.84 MHz)



(1) IMD uncorrected: −32.1 dBc (lower), −33.7 dBc (upper).

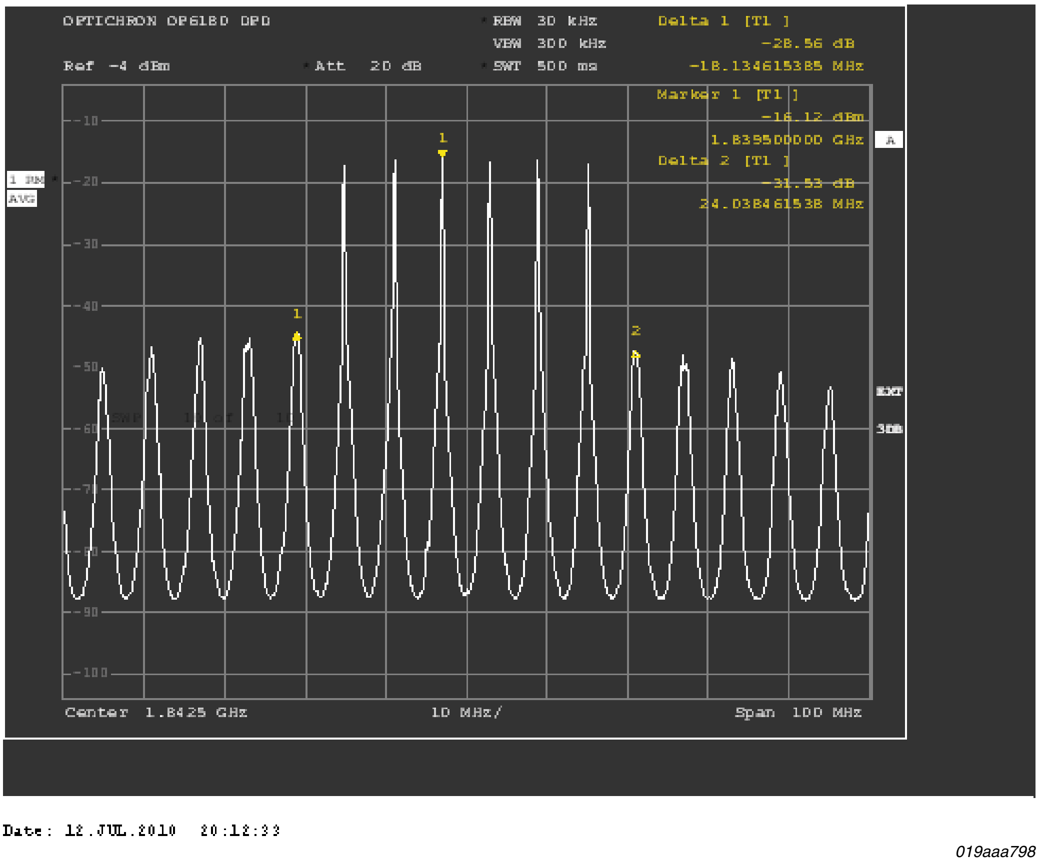
(2) IMD corrected: −52.1 dBc (lower), −52.6 dBc (upper).

Fig 19. DPD measurement, f_c = 1.88 GHz

4.3 DPD measurements with 6-carrier GMSK

The DPD measurements were performed using an Optichron OP6180 DPD system under the following conditions:

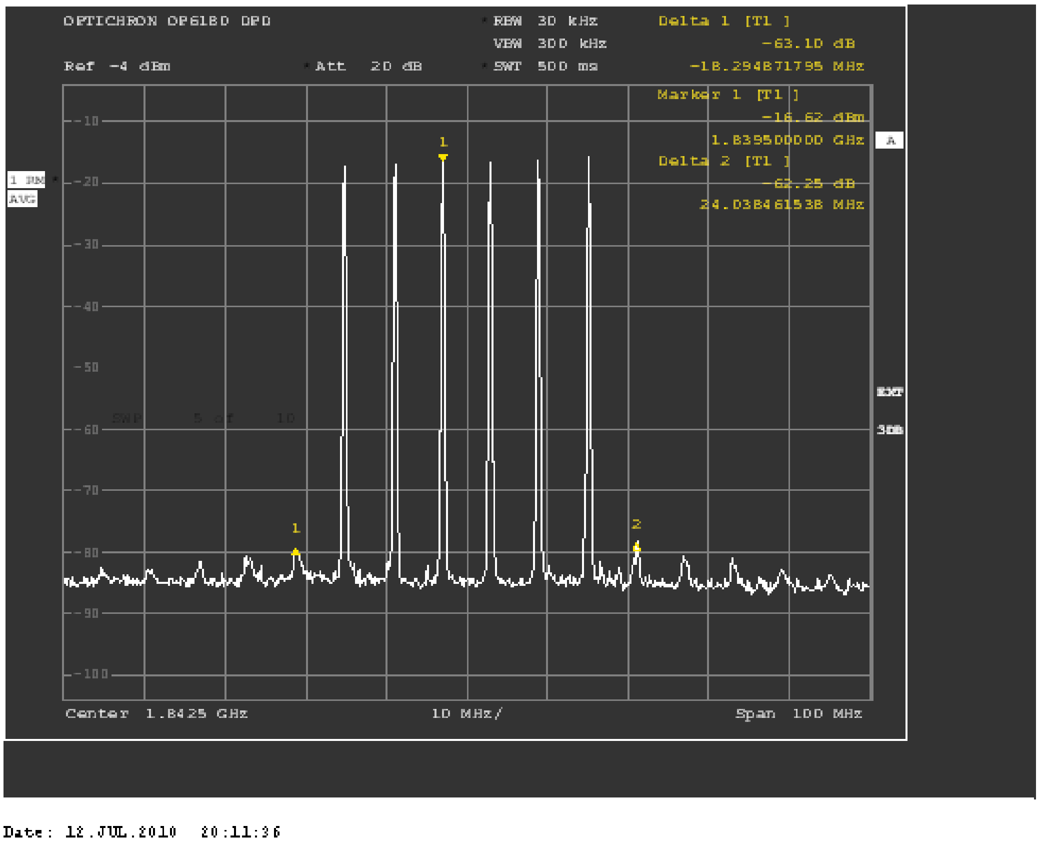
- 6-carrier GMSK signal, spacing: 6 MHz, peak-to-average ratio (PAR) = 6.2 dB at 0.01 % probability (total signal)
- f_c = 1.8425 GHz
- P_L = 47.2 dBm



Lower: –28.6 dBc.

Upper: –31.5 dBc.

Fig 20. 6-carrier GMSK DPD measurement, without DPD



019aaa799

Lower: –63.1 dBc.

Upper: –62.3 dBc.

Fig 21. 6-carrier GMSK DPD measurement, with DPD

5. BLF7G20LS-90P and BLF7G21LS-160P asymmetrical Doherty amplifier board

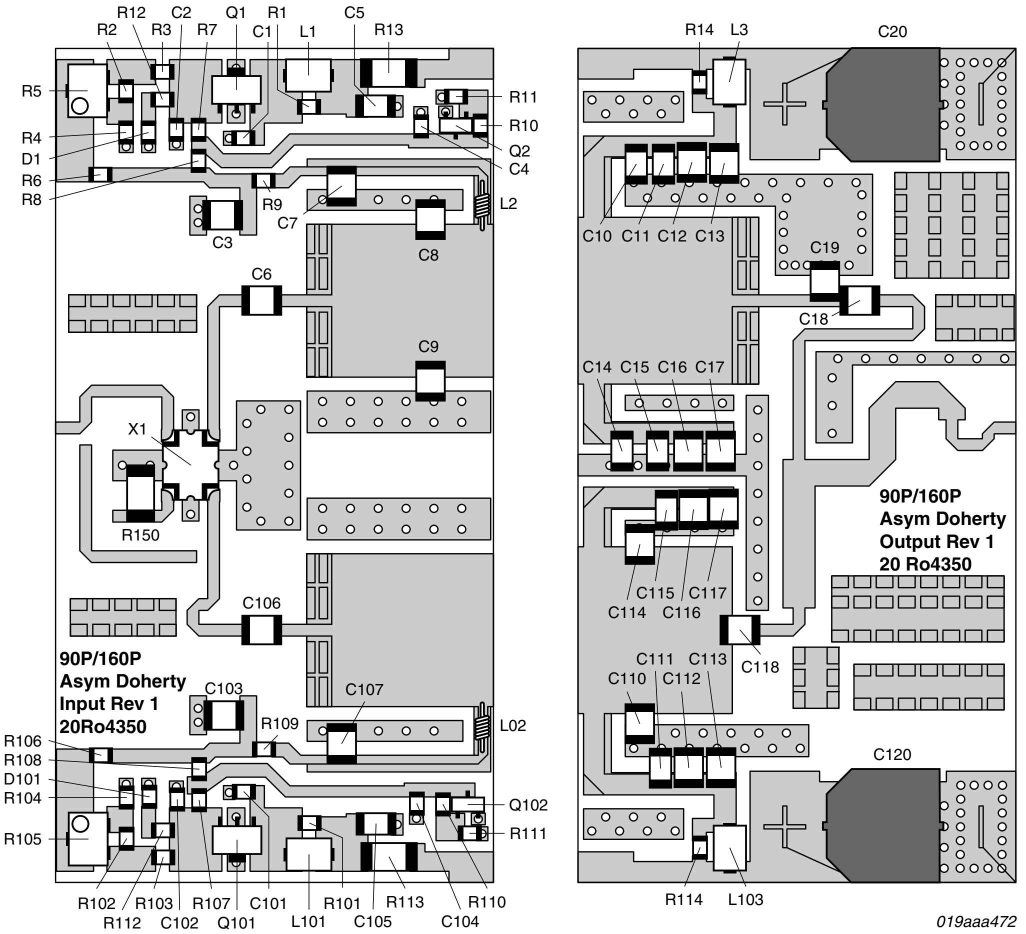


Fig 22. BLF7G20LS-90P and BLF7G21LS-160P asymmetrical Doherty amplifier board component layout

5.1 BLF7G20LS-90P and BLF7G21LS-160P asymmetrical Doherty amplifier board components

Table 1. BLF7G20LS-90P and BLF7G21LS-160P asymmetrical Doherty amplifier board components

Designator	Description	Part identifier	Manufacturer
Input PCB Output PCB	Rogers 4350; ε_r = 3.5; thickness 0.51 mm (0.020”)	-	Ohio circuits
C1, C2, C4, C101, C102, C104	100 nF ceramic 0805 capacitor	S0805W104K1HRN-P4	Multicomp
C3, C5, C10, C14, C103, C105	1 μF ceramic capacitor	GRM31CR72A105KA0	MuRata
C6, C7, C12, C16, C18, C106, C107, C112, C116, C118	30 pF ceramic chip capacitor	100B	American Technical Ceramics
C8, C9	0.9 pF capacitor	100B	American Technical Ceramics
C11, C15, C111, C115	100 nF capacitor	GRM31CR72E104KW03L	MuRata
C13, C17, C113, C117	10 μF capacitor	100B	MuRata
C19	1.1 pF capacitor	100B	MuRata
C20, C120	220 μF, 50 V electrolytic SMT capacitor	PCE3474CT-ND	Panasonic
C110	1.7 pF capacitor	100B	American Technical Ceramics
C114	1.6 pF capacitor	100B	American Technical Ceramics
L1, L3, L101, L103	Ferroxcube bead	2743019447	Fair Rite
L2, L102	10 nH inductor	0603CS-10NXJB	Coilcraft
Q1, Q101	78L08 voltage regulator	NJM#78L08UA-ND	NJR
Q2, Q102	2N2222 NPN transistor	MMBT2222	Fairchild
R1, R14, R101, R114	9.1 Ω resistor	CRCW08059R09FKEA	Vishay Dale
R2, R3, R102, R103, R106	430 Ω resistor	CRCW0805432RFKEA	Vishay Dale
R4	75 Ω resistor	CRCW080575R0FKEA	Vishay Dale
R104	0 Ω resistor	CRCW08050R0FKEA	Vishay Dale
R5, R105	200 Ω potentiometer	3214W-1-201E	Bourns
R6	2 kΩ resistor	CRCW08052K00FKTA	Vishay Dale
R7, R107	1.1 kΩ resistor	CRCW08051K10FKEA	Vishay Dale
R8, R108	11 kΩ resistor	CRCW080511K0FKEA	Vishay Dale
R9, R109	5.1 Ω resistor	CRCW08055R11FKEA	Vishay Dale
R10, R110	5.1 kΩ resistor	CRCW08055K10FKTA	Vishay Dale
R11, R111	910 Ω resistor	CRCW0805909RFKTA	Vishay Dale

Table 1. BLF7G20LS-90P and BLF7G21LS-160P asymmetrical Doherty amplifier board components *...continued*

Designator	Description	Part identifier	Manufacturer
R12, R112	1.1 kΩ resistor	CRCW08051K10FKEA	Vishay Dale
R13, R113	499 Ω/0.5 W resistor	CRCW2010499RFKEF	Vishay Dale
R150	EMC SMT 2010 50 Ω load	-	EMC
X1	5 dB hybrid coupler	X3C19P1-05S	Anaren

6. Abbreviations

Table 2. Abbreviations

Acronym	Description
ACPR	Adjacent Channel Power Ratio
CCDF	Complementary Cumulative Distribution Function
DPD	Digital PreDistortion
GSM	Global System for Mobile communications
GMSK	Gaussian Minimum Shift Keying
IBW	Integration BandWidth
IMD	InterModulation Distortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long-Term Evolution
MOSFET	Metal-Oxide Silicon Field-Effect Transistor
PAR	Peak-to-Average power Ratio
PCB	Printed-Circuit Board
W-CDMA	Wideband Code Division Multiple Access

7. Legal information

7.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

7.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

8. Contents

Date of release: 10 December 2010
Document identifier: AN10951